TE0720 TRM

Revision v.106

Exported on 2025-05-23

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Current online version of this document.

4 Overview

The Trenz Electronic TE0720 is an industrial-grade SoM (System on Module) based on AMD Zynq-7000 SoC with DDR3/DDR3L SDRAM, SPI flash memory, Gigabit Ethernet PHY transceiver, USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via high-speed stacking connections.

Refer to http://trenz.org/te0720-info for current online available documentation.

4.1 Key Features

- **SoC**
  - AMD XC7Z SoC: XC7Z014S / XC7Z020 [1)]
  - Speedgrade: -1 / -1L / -2 / -3 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: CLG484
- **RAM/Storage**
  - 1 GByte DDR3/DDR3L SDRAM [1)]
  - 32 MByte QSPI Flash Memory [1)]
  - 32 GB e.MMC system storage [1) 2)]
  - EEPROM with MAC address [3)]
- **On Board**
  - Gigabit Ethernet transceiver PHY
  - USB 2.0 ULPI transceiver
  - Power Supervisor with Watchdog Timer
  - System Controller (SC)
  - Serial EEPROM with EUI-48™ node identity / MAC address [3)]
  - Atmel CryptoAuthentication IC
  - Real time clock (RTC) [2)]
  - 3-axis accelerometer and magnetometer (eCompass) [2)]
  - 2 x User LED
  - FPGA DONE LED
  - 3 x Oscillator (FPGA, Ethernet, USB)
- **Interface**
  - 3 x B2B Connector (Samtec LSHM) for Trenz 4 x 5 SoM socket
    - PL: 152 HR IOs
    - PS: 14 x MIOs
- **Power**
  - Single 3.3 V or dual 5 V / 3.3 V power supply via B2B Connector
- **Dimension**
  - 40 mm x 50 mm
- **Notes**

  [1)] Assembly variant dependent.

  [2)] Not equipped on all variants.

  [3)] MAC address is write protected. 1,536 bits of storage space.

4.2 Block Diagram

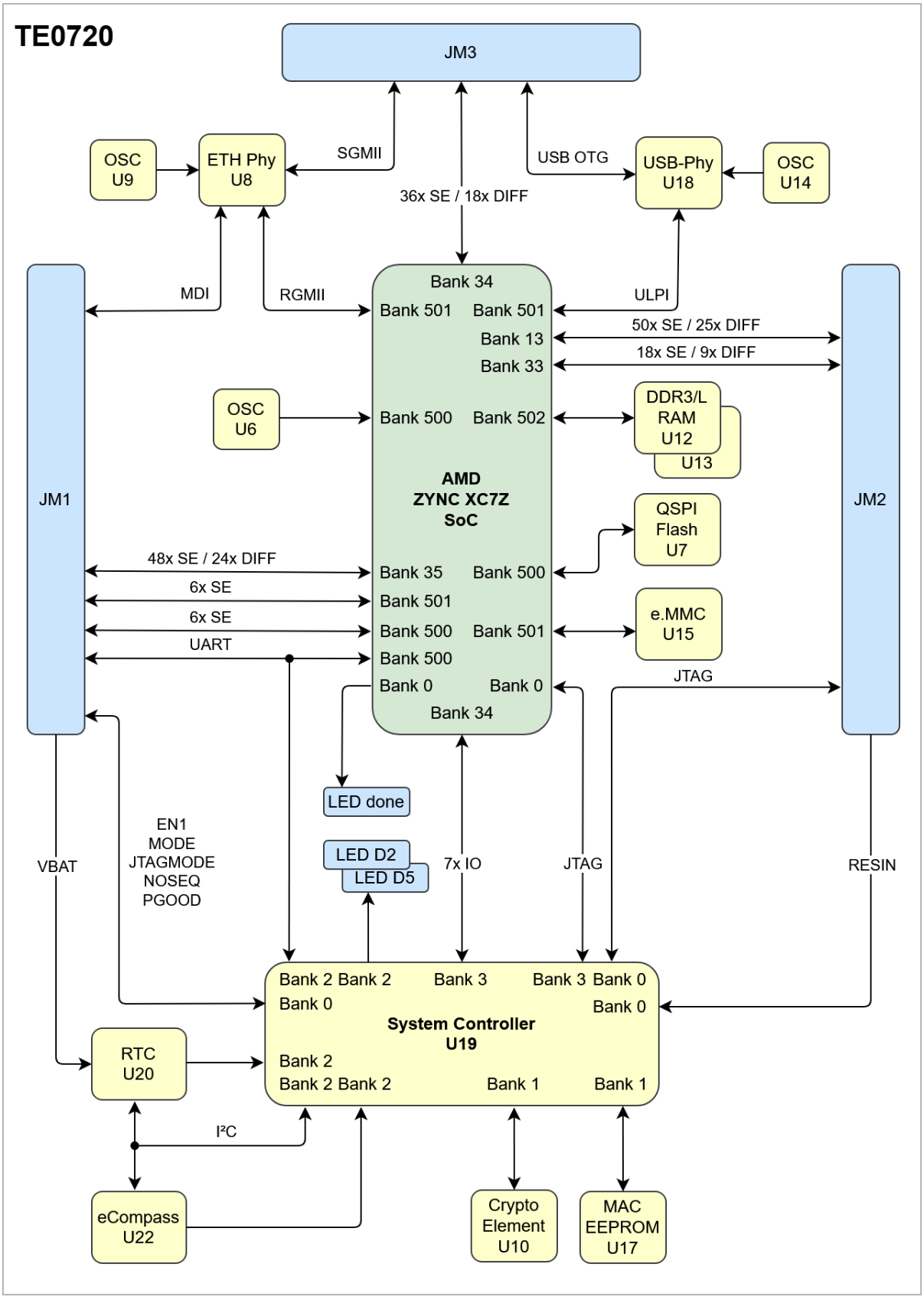

Figure 1: TE0720 block diagram

4.3 Main Components

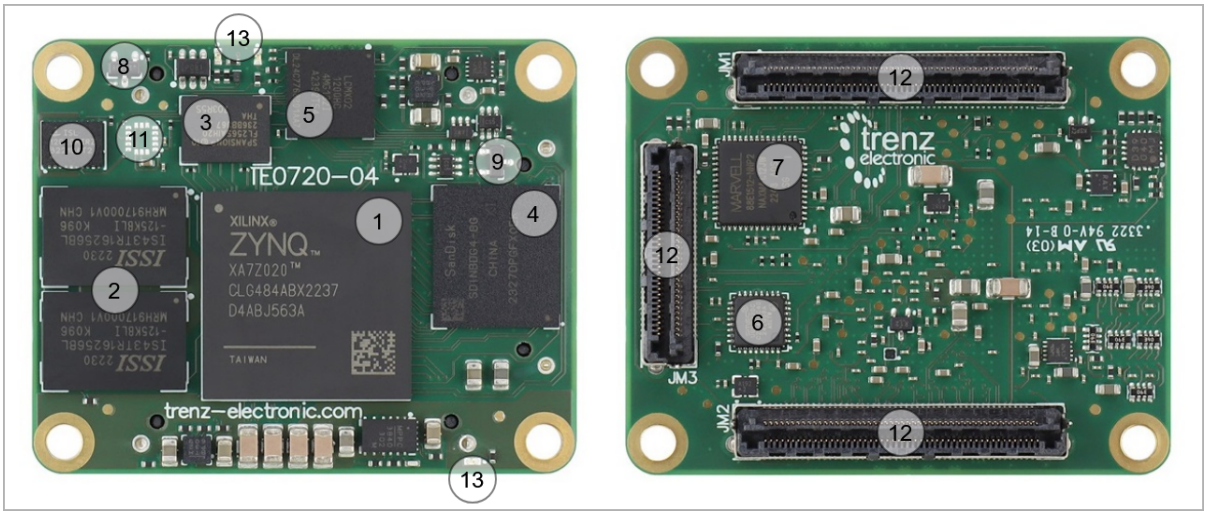

Figure 2: TE0720 main components

1. AMD Zynq XC7Z SoC, U5
2. DDR3/DDR3L SDRAM, U12, U13
3. Quad SPI Flash memory, U7
4. eMMC NAND Flash, U15
5. System Controller, U19
6. USB 2.0 ULPI transceiver, U18
7. Gigabit Ethernet transceiver, U8
8. Microchip CryptoAuthentication chip, U10
9. EEPROM with EUI-48™ node identity, U17
10. RTC, U20
11. eCompass, U22
12. B2B connector Samtec Razor Beam™ LSHM, JM1, JM2, JM3
13. LEDs, D2 & D5, D4

4.4 Initial Delivery State

Storage device name	Content	Notes
System Controller, U19	standard firmware	Visit TE0720 CPLD Firmware for further information.
eMMC, U15	not programmed	
SPI Flash, U7	not programmed	

Storage device name	Content	Notes
2 kBit EEPROM, U17	not programmed besides factory programmed MAC address	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	JM1	HR IO	48	
B2B	JM1	PS IO	6	Bank 501 voltage level is 1.8 V. SDIO or optional MIO (MIO40/.../MIO45).
B2B	JM1	PS IO	4	Bank 500 voltage level is 3.3 V (MIO0/MIO9/ MIO12/MIO13).
B2B	JM1	UART	2	Bank 500/SC Bank 2 voltage level is 3.3 V. UART or MIO (MIO14/ MIO15).
B2B	JM1	I2C	2	Bank 500 voltage level is 3.3 V . I^2C or optional MIO (MIO10/MIO11).
B2B	JM1	VBat	1	
B2B	JM1	ETH MDI	8	
B2B	JM2	HR IO	50	
B2B	JM2	HR IO	18	
B2B	JM2	JTAG	4	
B2B	JM3	ETH MDI	4	

Connector Type	Designator	Interface	IO CNT	Notes
B2B	JM3	USB OTG	3	
B2B	JM3	USB OTG VBus	2	
B2B	JM3	HR IO	36	

Table 2: Board Connectors

5.2 Test Points

Test Point	Signal	Notes
TP1	1V	
TP2	VIN	
TP3	1.5V	
TP4	1.8V	
TP5	VTT	
TP6	VTTREF	
TP7	3.3VIN	
TP8	3.3V	
TP9	VCCIO13	
TP10	VCCIO33	
TP11	VCCIO34	
TP12	VCCIO35	

Test Point	Signal	Notes
TP13	AVCC	
TP14	AVREF	
TP15	AGND	
TP16	GND	
TP17	GND	
TP18	GND	
TP19	GND	
TP20	GND	
TP21	PS-RST	
TP22	PROG_B	
TP23	PS-CLK	
TP24	PS-CS	
TP25	SPI-SCK/M4	
TP26	SPI-DQO/MO	
TP27	SPI-DQ3/M3	
TP28	SPI-DQ2/M2	
TP29	SPI-DQ1/M1	
TP30	VBATT	
TP31	PS-POR-B	

Test Point	Signal	Notes
TP32	PS-RST	

Table 3: Test Points Information

6 On-board Peripherals

Chip/ Interface	Designator	Connected to	Notes
SoC	U5	• SC • JM1, JM2, JM3 • ETH PHY • USB PHY • Power Supervisor	
RAM	U12, U13	• AMD Zynq SoC DDR Interface PS Bank 502	
Quad SPI	U7	• AMD Zynq SoC Bank 500	
e.MMC	U15	• AMD Zynq SoC Bank 501	
USB 2.0 ULPI PHY	U18	• AMD Zynq SoC Bank 501	
ETH PHY	U8	• AMD Zynq SoC Bank 501	
SC	U19	• JM1, JM3 • MAC EEPROM • RTC • Crypto Element • eCompass • Power Supervisor • System Supervisor	Visit TE0720 CPLD Firmware for further information.

Chip/ Interface	Designator	Connected to	Notes
MAC EEPROM	U17	• SC	Contains pre-programmed globally unique 48-bit node address.
RTC Real time clock	U20	• SC • eCompass • Crypto Element	Battery backed functionality via VBat pin. I^2C adresses: Registers 0x6F/RAM 0x57.
Crypto Element	U10	• SC • eCompass • RTC	
eCompass	U22	• SC • RTC • Crypto Element	I^2C adresses: 0x1D
Power Supervisor	U26	• SC • AMD Zynq SoC	
Power Supervisor	U27	• SC	
Oscillator	U6	• Zynq SoC PS Bank 500	33.3 MHz
Oscillator	U14	• USB PHY	25 MHz
Oscillator	U9	• ETH PHY	52 MHz

Table 4: On board peripherals

7 Configuration and System Control Signals

Signal Name	Connector.Pin	Direction[1)]	Description
NOSEQ	JM1.7	INOUT	Module Power management [2) 3) 4)].
EN1	JM1.28	IN	Power enable signal [2) 3) 4)].
PGOOD	JM1.30	INOUT	Power good and/or Boot mode select signal [2) 4)]
MODE	JM1.32	IN	Boot mode select signal [2) 3) 4)].
JTAGMODE	JM1.89	IN	Select JTAG target on the SoM [2) 3) 4)].
RESIN	JM2.18	IN	Reset signal [4)].
VBUS_V_EN	JM3.53	OUT	Enables USB Host Bus Voltage
USB-VBUS	JM3.55	IN	Detects USB Host Bus Voltage
MIO14/ MIO15	JM1.92 / JM1.85	INOUT	UART to SoC and SC [2)]
MIO10/ MIO11	JM1.95 / JM1.93	INOUT	I^2C SoC to B2B
X5 / X7	U5C.P22 / U5C.N22 U19D.J1 / U19D.M1	INOUT	I^2C SC to SoC

Signal Name	Connector.Pin	Direction[1)]	Description
SDA / SCL	U22.6 / U22.4 U20.12 / U20.11 U10.1 U16C.P7 / U16C.P8	INOUT	I^2C SC to RTC, eCompass and Crypto Element

Table 5: Controller signal.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2)] Firmware dependent. Refer to TE0720 CPLD Firmware for further information.

[3)] Do not leave floating.

[4)] For more information refer to 4 x 5 SoM Integration Guide.

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name / Schematic Name	Connector.Pin	Direction [1)]	Note
VIN	JM1.1 / JM1.3 / JM1.5 / JM2.4 / JM2.4 / JM2.6 / JM2.8	IN	Supply voltage from carrier.
3.3VIN	JM1.13 / JM1.15 / JM2.91	IN	Supply voltage from carrier.
3.3VIN / VREF_JTAG	JM2.91	OUT	JTAG reference voltage.
VCCIO13	JM2.7 / JM2.9	IN	SoC IO Bank supply from carrier.
VCCIO33	JM2.5	IN	SoC IO Bank supply from carrier.
VCCIO34	JM2.1 / JM2.3	IN	SoC IO Bank supply from carrier. VCCIO34 must be connected to power even if this bank is not used.
VCCIO35	JM1.9 / JM1.11	IN	SoC IO Bank supply from carrier.
VBAT_IN	JM1.79	IN	RTC battery buffer supply
3.3V	JM2.10 / JM2.1	OUT	
1.8V	JM1.39	OUT	

Power Rail Name / Schematic Name	Connector.Pin	Direction [1]	Note
1.5V [2]	JM2.19	OUT	

Table 6: Module power rails.

[1] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2] For SoM variants with DDR3L RAM, this voltage is reduced to 1.35 V. On these variants, resistor R39 has a value of 120 kΩ instead of 100 kΩ for 1.5 V variants.

8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
1	-	-	-	Configuration signal setup.	See Configuration and System Control Signals.
	3.3VIN VIN	_ [1]	- -	Main Power supply.	
2	EN1	3.3 V (± 5 %)	_ [2]	Enable SoM.[3]	
3	3.3V or 1.8V	_ [1]	-	Module generated output voltages.	SoM's internal power-on sequence is complete when these voltages reach their nominal values.
4	VCCIO 35 VCCIO 34 VCCIO 33 VCCIO 13	_ [1]	-	Supply module bank voltages. [4]	

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
5	PGOOD	3.3 V (± 5 %)	_ [3]	SoM power good signal.	All power sources are stable.

Table 7: Baseboard Design Hints

[1] Refer to Recommended Operating Conditions.

[2] Firmware dependent. Refer to TE0720 CPLD Firmware for further information.

[3] Do not assert signal before input power supply reached 90 % of nominal value.

[4] VCCIO34 needs to be connected to power even if bank is not used, to setup startup parameters.

For more information refer to DS187.

9 Board to Board Connectors

> These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

9.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Table 8: Connectors.
The module can be manufactured using other connectors upon request.

9.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Table 9: Speed rating.

9.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

9.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

10 Technical Specifications

This TRM is generic for all variants.

- The voltage ranges are generally the same across variants (exceptions are possible, depending on custom requests).
- The temperature range can differ depending on the assembly version.
- The combination of a carrier and a SoM might have different requirements.

Variants of modules are described here: Article Number Information. Please contact us to inquire options.

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VIN	Supply voltage from carrier.	-0.3	6	V
3.3VIN	Supply voltage from carrier.	-0.5	3.6	V
VCCIO13	SoC IO Bank supply from carrier.	-0.5	3.6	V
VCCIO33	SoC IO Bank supply from carrier.	-0.5	3.6	V
VCCIO34	SoC IO Bank supply from carrier.	-0.5	3.6	V
VCCIO35	SoC IO Bank supply from carrier.	-0.5	3.6	V
VBAT_IN	RTC battery buffer supply.	-0.3	6	V

Table 10: Absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be different in dependence to the assembly variant. The voltage ranges should not be affected by assembly variants (exceptions are possible, depending on custom request).

Trenz Electronic classifies modules into temperature range categories by subsumption of its component data (PCB, ICs, connectors, passive components). The temperature ranges are values for ambient air temperature and do not reflect the junction temperature of individual components.

The categories are:

- Modules with commercial temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 75 °C.
- Modules with extended temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 85 °C.
- Modules with industrial temperature grade are equipped with components that cover at least the ambient temperature range of -40 °C to 85 °C.

These categories do not take into account the entire custom system consisting of:

- Customer SoC/FPGA design.
- Cooling solution, active and or passive cooling.
- Climate or enviromental conditions besides ambient temperature range.
- Module orientation, neighboring assemblies, neither other heat sources nor the SoC/FPGA as heat source to other components.

10.2.1 Temperature range

This SoM is capable of being operated at industrial-grade temperatures, which cover at least the range of -40 °C to 85 °C.

The temperature of individual components should not exceed the specified range due to self-heating or heating by adjacent components.

The Operating temperature range depends also on customer design and cooling solution. Consult Cooling Solutions for more information.

10.2.2 Voltage rails

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VIN	Supply voltage from carrier.	3.15	5.25	V
3.3VIN	Supply voltage from carrier.	3.15	3.45	V
VCCIO13	SoC IO Bank supply from carrier.	1.14	3.465	V

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VCCIO33	SoC IO Bank supply from carrier.	1.14	3.465	V
VCCIO34	SoC IO Bank supply from carrier.	1.425	3.465	V
VCCIO35	SoC IO Bank supply from carrier.	1.14	3.465	V
VBAT_IN	RTC battery buffer supply.	2.5	5.0	V

Table 11: Recommended operating conditions.

10.3 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.
- PCB thickness: 1.6 mm ±10 %.

All dimensions are given in millimeters.

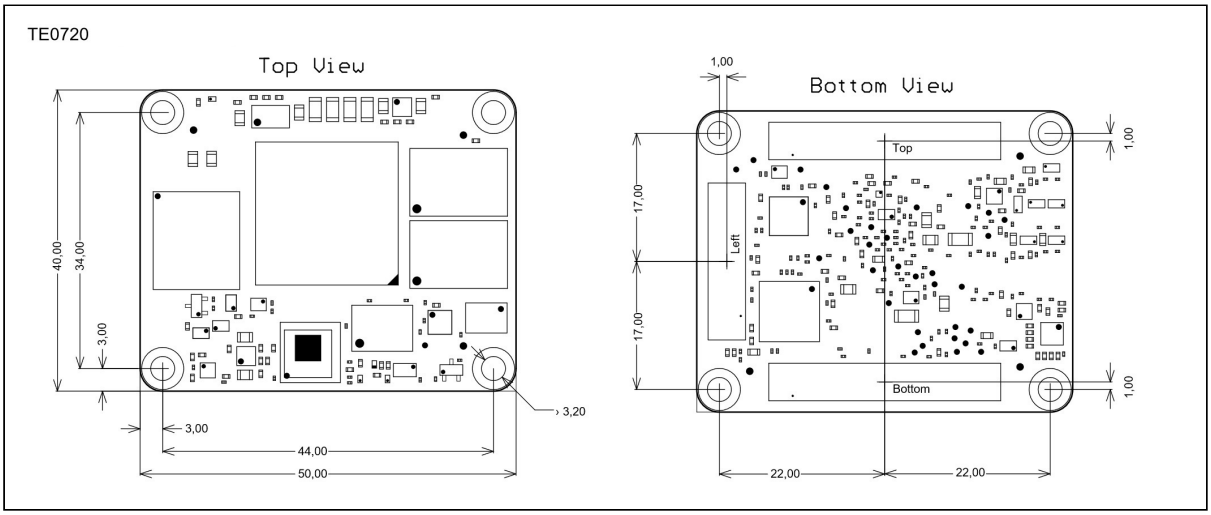

Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0720 overview page	
English page	German page

Table 12: Trenz Electronic Shop Overview

12 Revision History

12.1 Hardware Revision History

The hardware revision number is on the PCB adjacent to the module identifier, separated by a dash.

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Links
2022-03	04	1. Revised power supply circuit, replaced next components: - EN6347QI (U1) by MPM3840GQV-Z, - EP53F8QI (U2, U3) by MPM3834CGPA, - TPS27082LDDCR (Q1) by MP5077GG-Z. 2. Added power supervisor BD39040MUF (U27). Next signal connected to system controller: - PG_All (U27 - U19.C12) with pull-up resistor R67; - WDEN (U27.13 - U19.C6) with pull-down resistor R80; - WDIN (U27.14 - U19.N8); - WDOUT (U27.16 - U19.M3). 3. Signal MIO8 (U5.E5) connected to system controller (U19.N7) 4. Added pull-down resistors R64 (net ON_1V0) and R65 (net ON_1V8) 5. Revised voltage supervisor U26 circuit: U26.6 (VDD) connected to 3.3VIN, Added protection diode D3 to U26.3 (#MR input) 6. Replaced BKP0603HS (L1, L2, L3, L4, L5, L7, L8) by MPZ0603S121HT000 7. Auxiliary information has been added on Samtec B2B connectors page 8. PCB: Revised layout of power supplies 9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected 10. PCB: Added option to install Heatsink SuperGrip (c) 11. Added capacitors C7, C8, C9 (100uF, 1V) 12. Changed voltage divider resistors (R21, R61) to set the threshold for U26. 13. Changed capacitor designator (C14) 14. Added note regarding VCCIO34, page B2B-Connectors	REV04 PCN-202202

Date	Revision	Changes	Documentation Links
2015-01	03	1. Bootmode is now latched on Reset 2. Fixed Xilinx "AR# 65240" . Added supervisor TPS3106K33DBVR (U26) according to Xilinx recommendations. 3. Replaced SiT8008AI-73-XXS-25.000000E with SiT8008AI-73-18S-25.000000E 4. Removed Hirose Ultra Small Coaxial Connector (J1) 5. Added Testpoints 6. System Controller updates to Revision 05 7. Change eMMC from MTFC32GAKAECN-3M to IS21ES32G-JCLI 8. Change DDR3 RAM (U12, U13) from IM4G16D3FABG-125I to IS43TR16256BL-125KBLI 9. All SoMs use S25FL256SAGBHI20 Flash (U7) 10. Change eMMC (U15) to IS21ES08G-JCLI 11. Clock Revision Change (U6, U14) SiT8008AI-... to SiT8008BI-... Firmware changes: 12. Added generic options for PUDC and Boot Mode 13. Set pin associated with MIO7 to Pullnone 14. Adding internal 3.3V enable signal en_3v3_int 15. Set JTAG C_* signals high impedance until 3.3V is enabled 16. Boot mode pins set to GND or high impedance until en_3v3_int is high 17. MIO14,15 high impedance until en_3v3_int is high 18. Improved JTAG time constraints 19. JTAG drive strength adjustment 20. Bugfix I2C to GPIO module (I2C_to_GPIO.v) 21. Changed Firmware Identifier to REV06 22. Change eMMC (U15) from IS21ES08G-JCLI / IS21ES32G-JCLI to SDINBDG4-8G-XI2 / SDINBDG4-32G-XI2 23. Change Ferrite Beads (L1, L2, L3, L4, L5, L7, L8) BKP0603HS121-T to MPZ0603S121HT000	REV03 PCN-202106 PCN-202101 PCN-202101 PCN-202001 PCN-201601 PCN-201503

Date	Revision	Changes	Documentation Links
2014-09	02	1. JTAG only boot mode is now supported 2. Winbond W25Q256FV SPI Flash memory replaced with Spansion S25FL256 3. Texas Instruments TPS51200 Sink/Source DDR Termination Regulator replaced with TPS51206 4. Changed MDIO pullup from 10k to 4k7 5. Changed eMMC core supply from switched 3.3Vout to 3.3Vin 6. MAC EEPROM power changed from 3.3V to 1.8V 7. I^2C Multiplexing no longer needed (to select between RTC and MEMS), all I2C devices are on the same bus. 8. ST LSM303DLM (e-compass: 3D accelerometer and 3D magnetometer) MEMS is no longer assembled in standard assembly variants 9. Removed test pads on top layer 10. Increased component clearance from mounting holes on bottom layer 11. System Controller in-system programming via B2B JTAG pins 12. JM1 pin 89 has new function that enables System Controller JTAG Chain no impact for old designs that connect this pin to GND	REV02 PCN-20140730
-	01	Prototypes	REV01

Table 13: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

12.2 Document Change History

Date	Revision	Contributors	Description
2025-05-23	v.106	ED	• Updated recommended minimum voltage for VCCIO34 to 1.425 V within section Recommended Operating Conditions. • Fix typos.

Date	Revision	Contributors	Description
2025-05-13	v.104	Kilian Jahn	• Updated to TRM version 4.2 • Updated TRM to hardware revision 04 • Fixed Inter Page Links • Updated PDF & PDF-Web Link
2021-11-15	v.95	John Hartfiel	• changed currently available chapter to new style
2021-06-21	v.93	Mohsen Chamanbaz	• fix typo for LED location on main component section
2019-02-05	v.92	John Hartfiel	• small document update
2018-07-05	v.89	John Hartfiel	• Update power rail section
2017-11-10	v.85	John Hartfiel	• Replace B2B connector section
2017-09-07	v.84	John Hartfiel	• Correction of Boot Mode section
2017-08-31	v.83	Jan Kumann	• Initial document.
--	all	Mohsen Chamanbaz , ED , John Hartfiel , Jan Kumann , Kilian Jahn , Martin Rohrmüller	• --

Table 25: Document change history table.

13 Disclaimer

13.1 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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